

Device leakage is increasing as geometry shrinks.

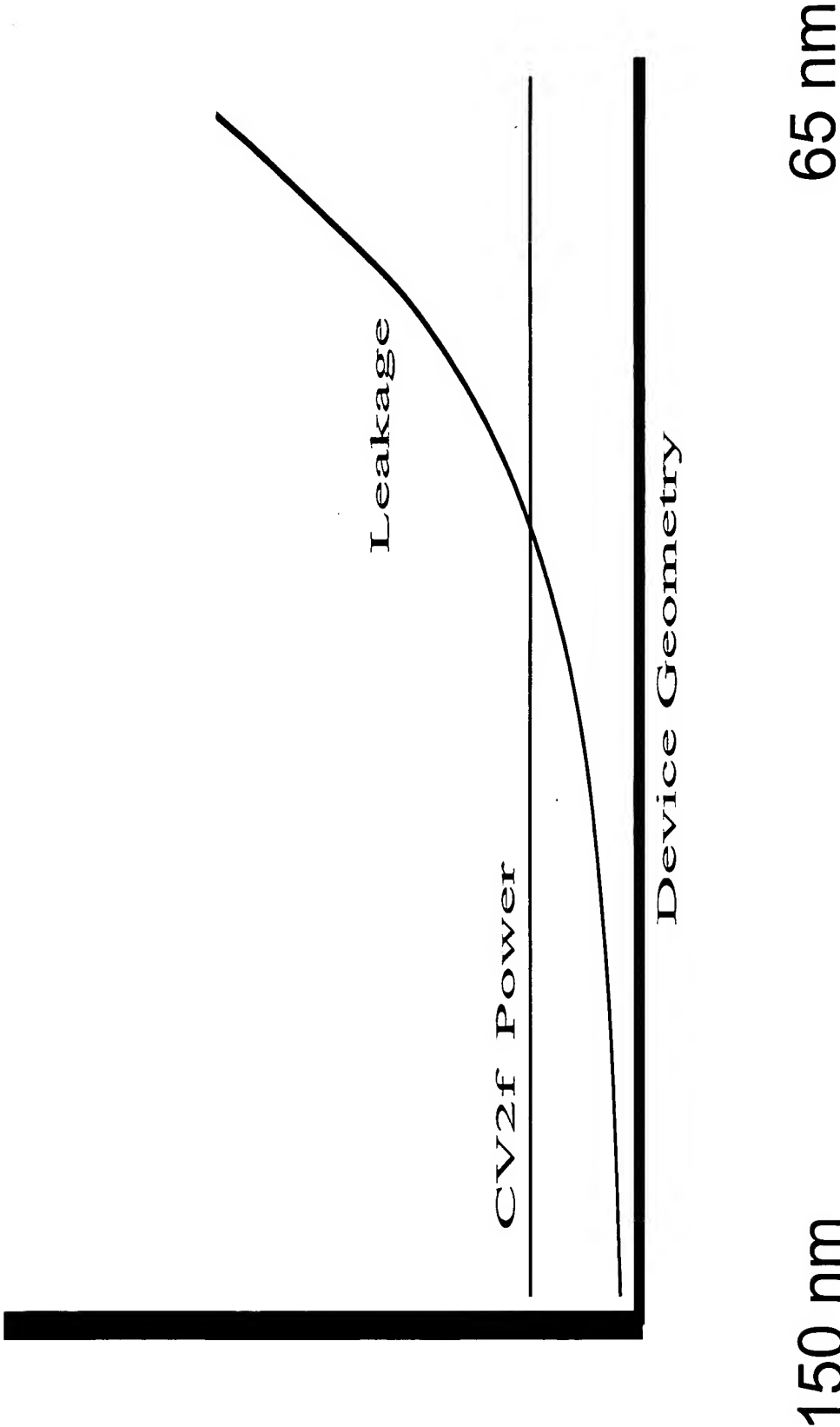
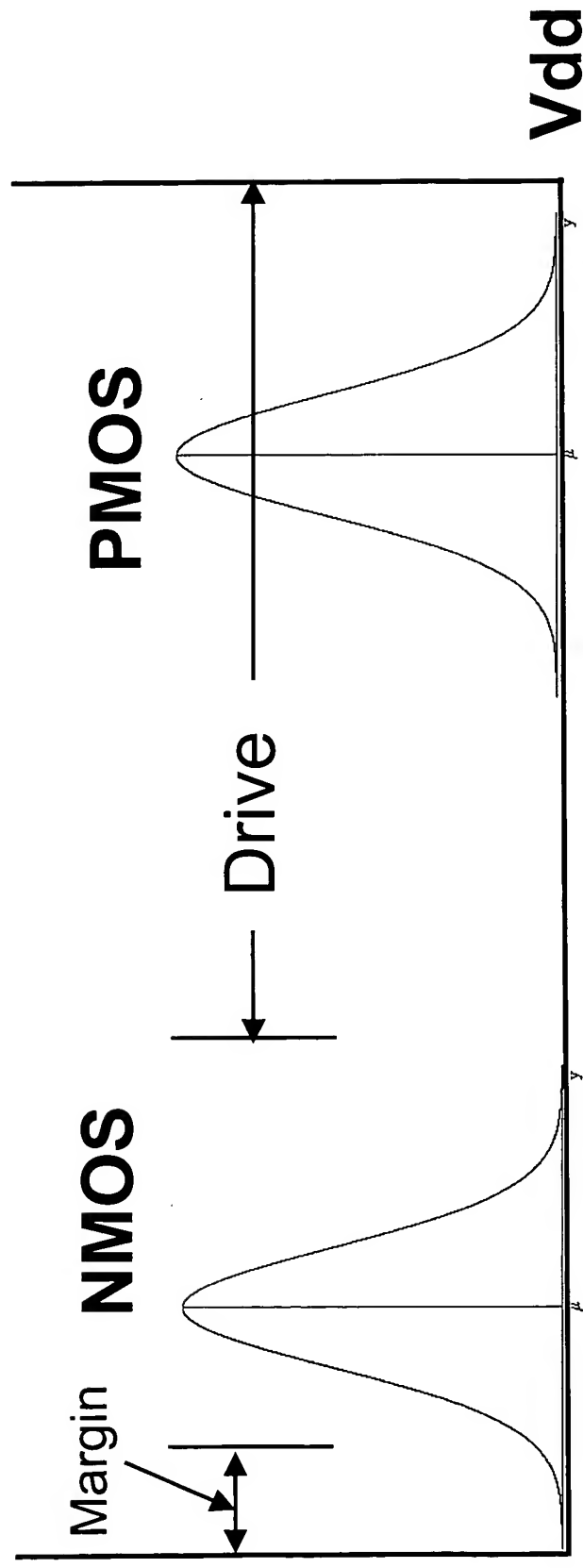


FIG. 1

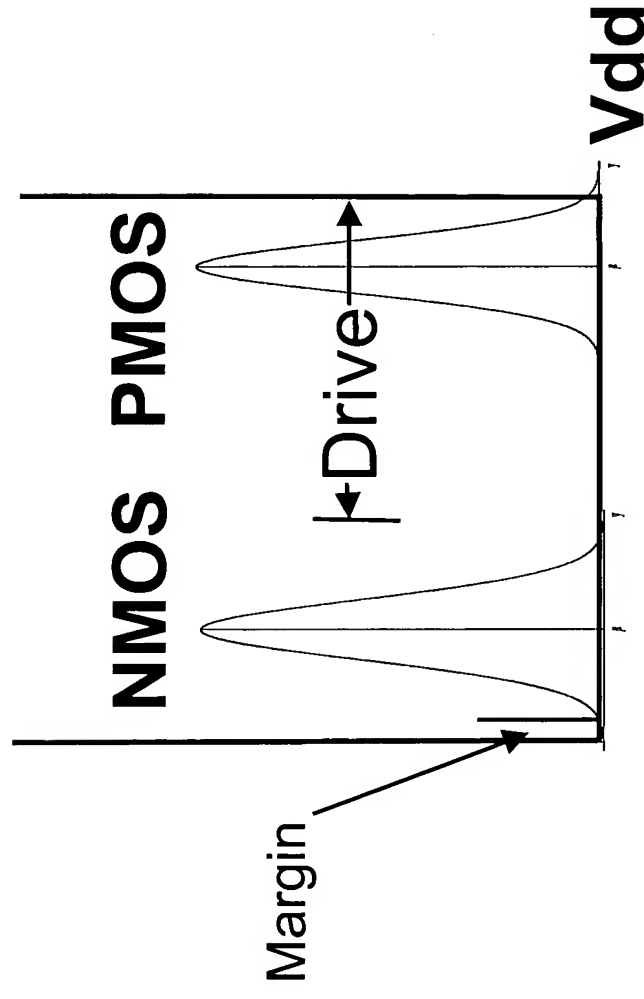
Margin vs. Drive Squeeze



Large Geometry V_t Distribution in the Power Supply Range

FIG. 2

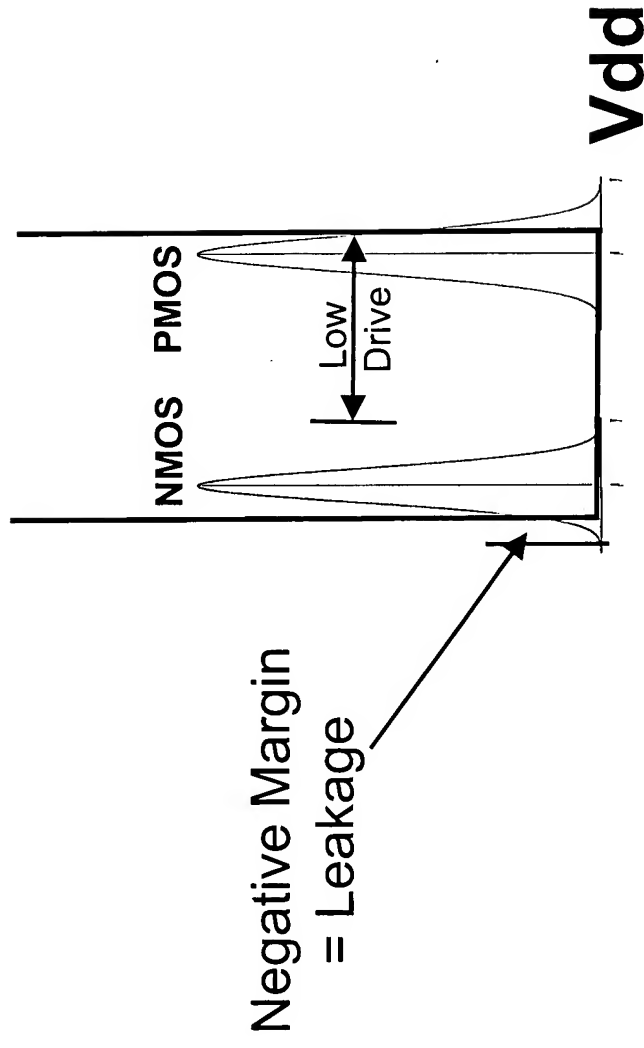
Margin vs. Drive Squeeze



Smaller Geometry V_t Distribution in the Power Supply Range

FIG. 3

Margin vs. Drive Squeeze



Small Geometry V_t Distribution in the Power Supply Range

FIG. 4

Passive Back Bias

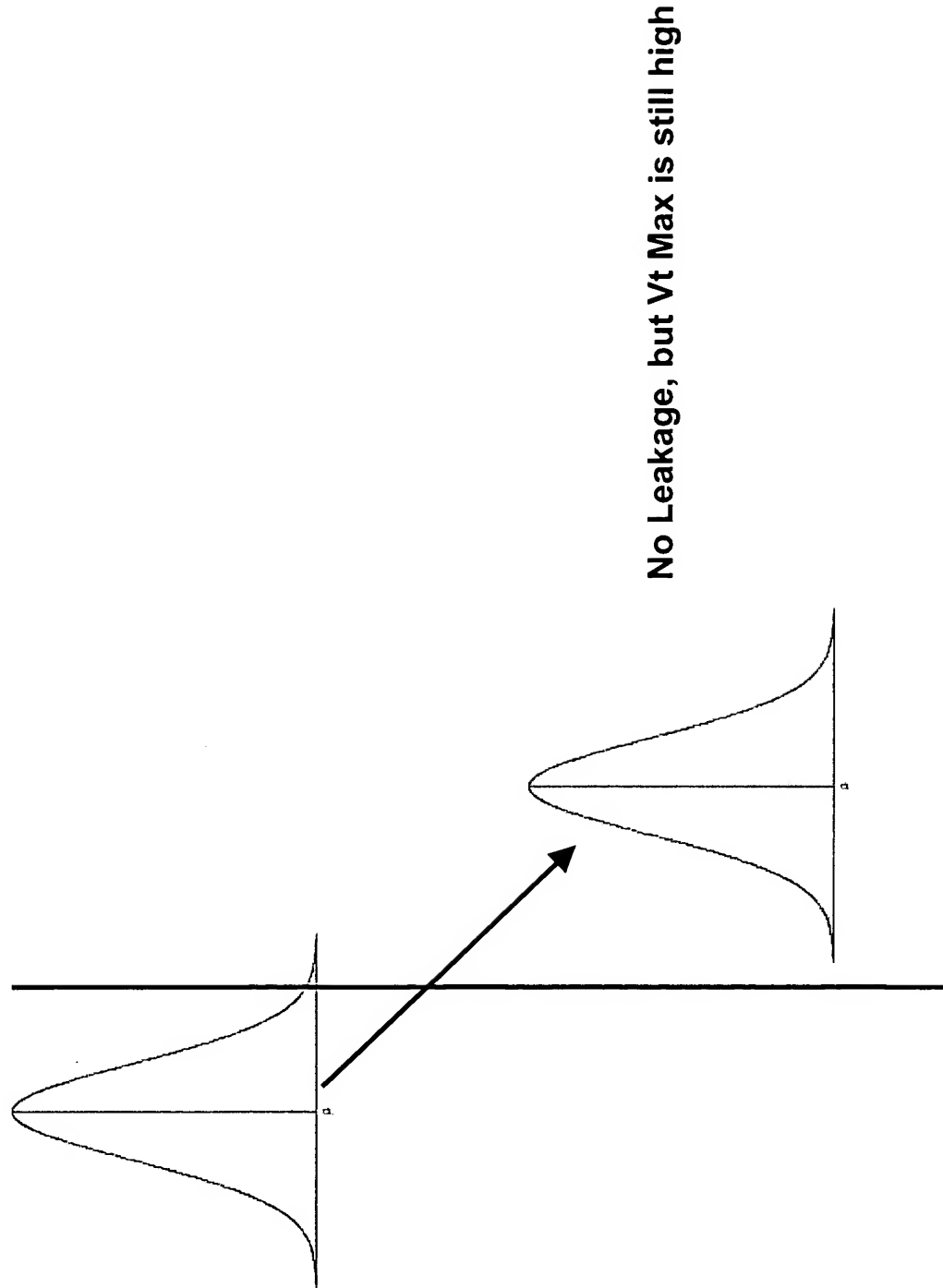
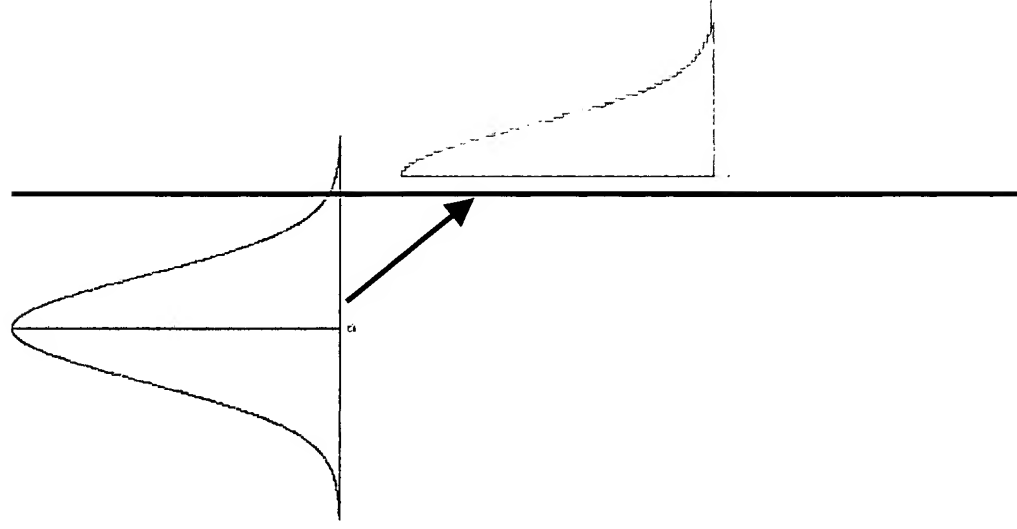


FIG. 5

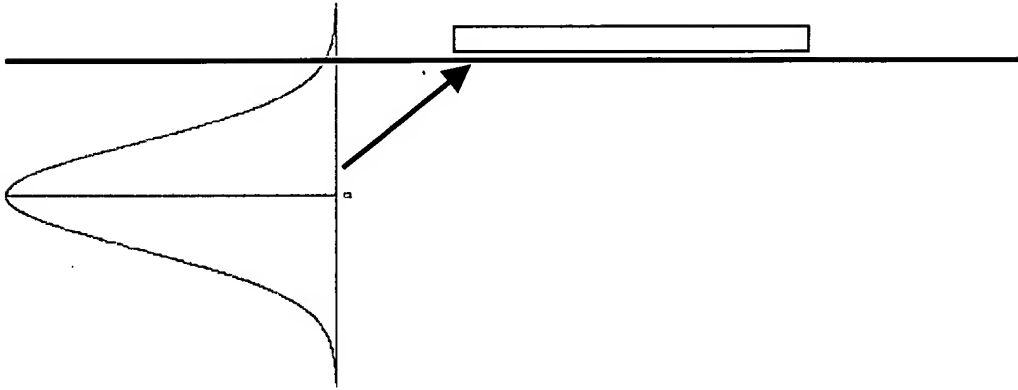
One bit Active Back Bias



No Leakage, but V_t Max is still high

FIG. 6

N-bit Active Back Bias

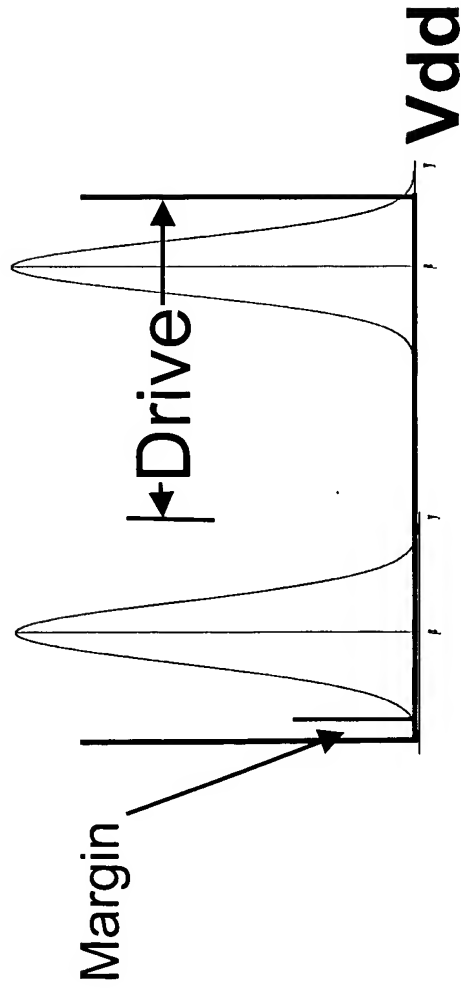


No Leakage, and V_t Max is greatly reduced

FIG. 7

Margin vs. Drive Squeeze

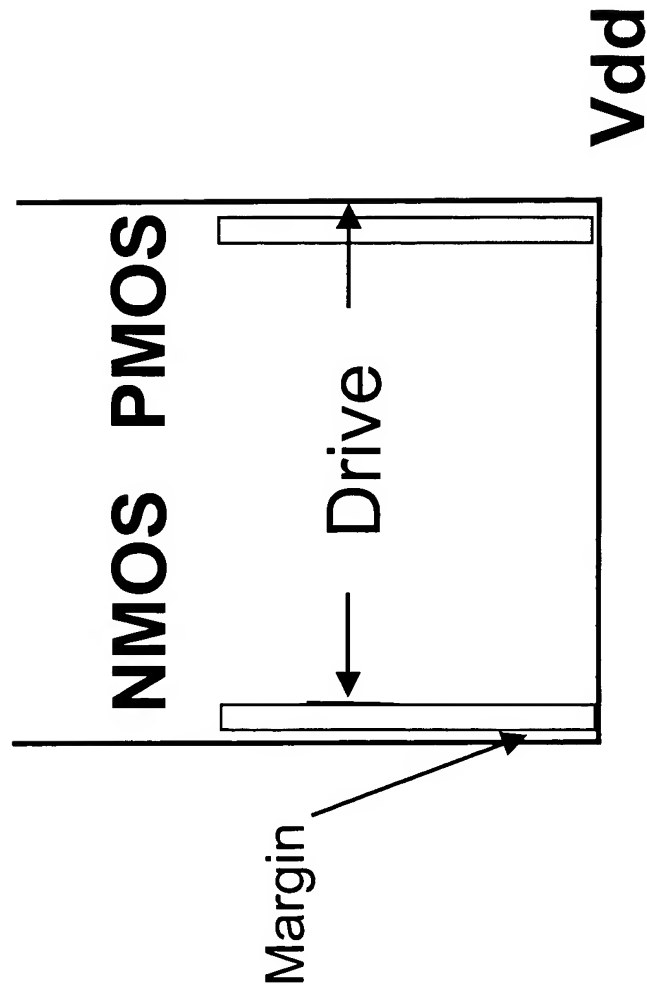
NMOS PMOS



Smaller Geometry Vt Distribution in the Power Supply Range

FIG. 8

Margin / Drive with N-bit Active Back Bias



Smaller Geometry V_t Distribution in the Power Supply Range with N-bit Active Back Bias

FIG. 9

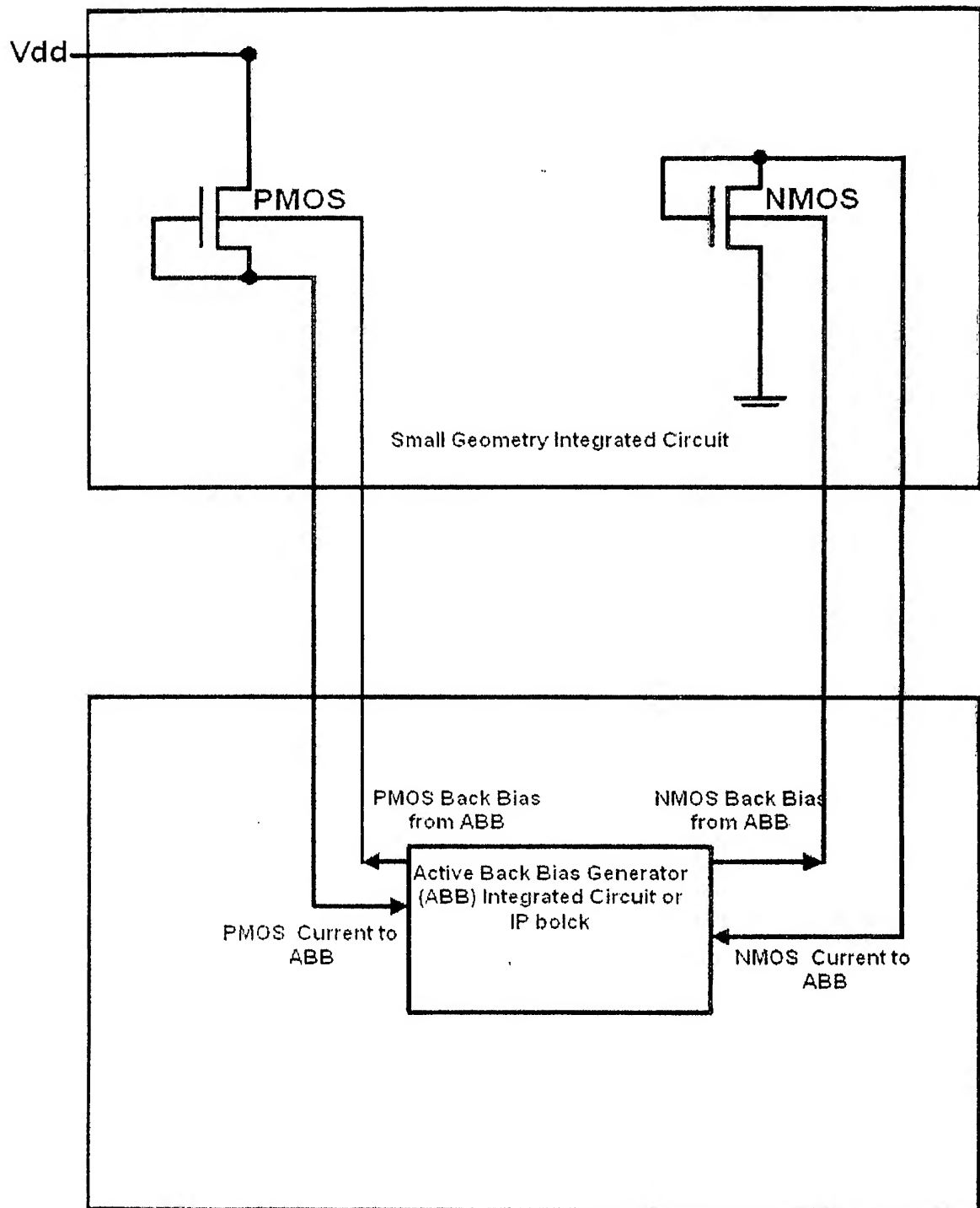


Fig. 10

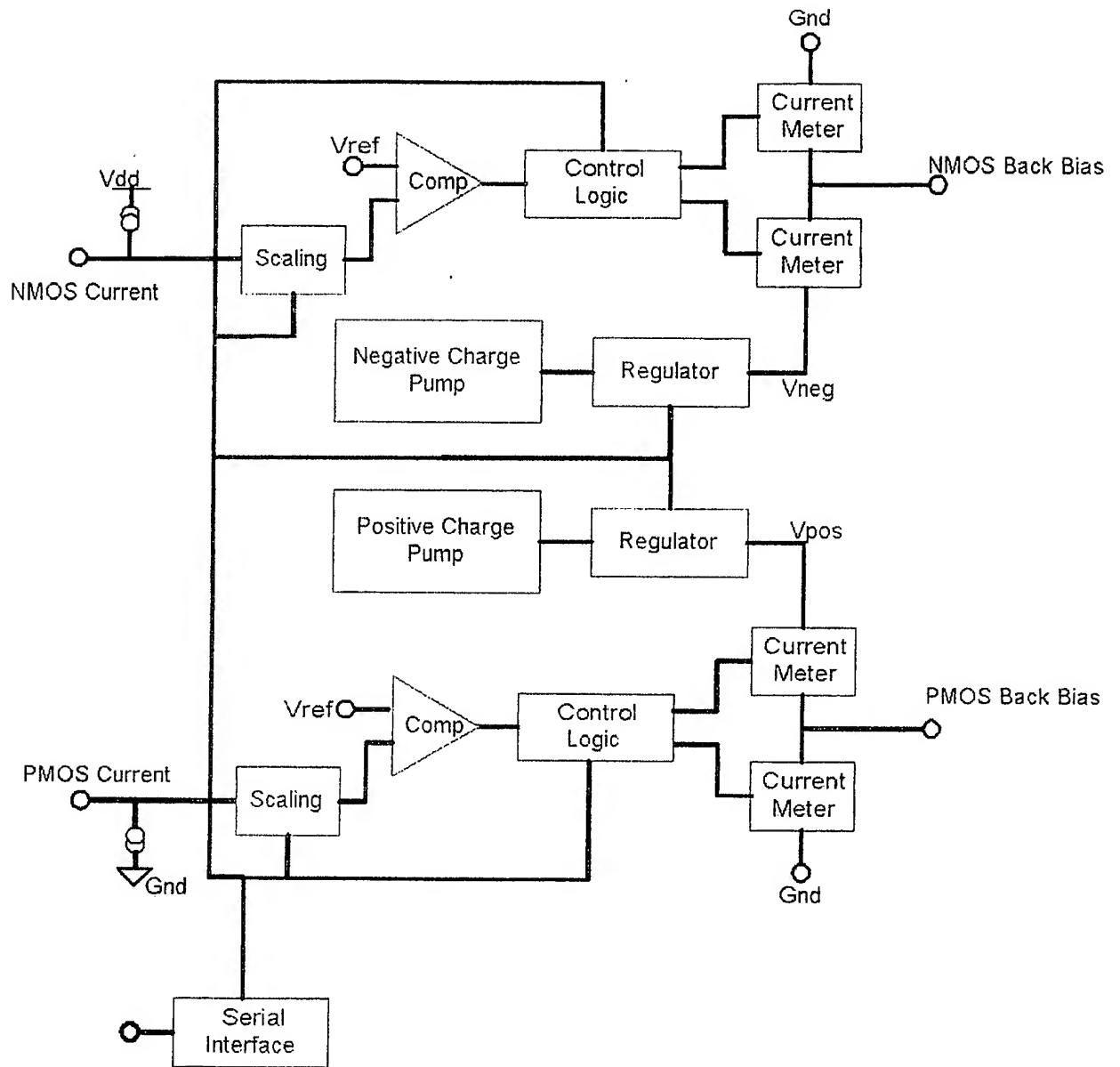


Fig. 11